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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Docket No.:	TI-31026
	Jonathan Brodsky, et al.	Art Unit:	2814
Serial No.:	09/668,999	Examiner:	Dana Farahani
Filed:	September 25, 2000	Date:	February 1, 2002

Confirmation No.: 3740

For: CIRCUIT AND METHOD FOR AN INTEGRATED CHARGED DEVICE MODEL CLAMP

Assistant Commissioner for
Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that on 2-1-02, this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Ann Trent
Ann Trent

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

Dear Sir:

Responsive to the Office Action dated November 2, 2001 (Paper No. 4), the six month statutory period for response having been shortened by three months and now being set to expire on February 4, 2002, please consider the following remarks.

REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-24 are in the case. All claims were rejected. No amendments have been made.

Applicants' attorney hereby thanks the Examiner for the telephone interview held on even date in which Applicants' attorney informed the Examiner that the above-mentioned Office Action arrived in the mails with two copies of Page One of the Notice

of References Cited, but with no copy of Page Two of such Notice and with no copy of any of the references cited in such Notice. In addition, in such interview the Examiner confirmed that the patent to Utsunomiya et al., cited in the rejection under 35 U.S.C. § 103(a), is U.S. Patent No. 6,207,996 B1. Finally, the Examiner agreed to send a copy of both pages of the above-mentioned Notice, as well as a copy of all of the references cited in such Notice. Applicants' attorney hereby notes, even though it was not discussed in such interview, that the Office Action Summary sheet in the above-mentioned Office Action received by Applicants has Box 8 checked, indicating a restriction requirement. However, it is understood that instead of Box 8, Box 6 should have been checked, since the remainder of such Office Action deals with rejections directed to all claims in the application, with no restriction or election being mentioned. In spite of the deficiencies in the form of the above-mentioned Office Action, Applicants hereby submit this Response, intended to be fully responsive to such Office Action, in order to expeditiously advance the prosecution of the above-identified application.

Regarding the rejection of Claims 1-17 and 21 under 35 U.S.C. § 102(e) as allegedly being anticipated by the patent to Pan, this rejection is respectfully traversed. The independent claims subject to this rejection are Claims 1, 10, 17 and 21. Regarding Claim 1, this claim recites an integrated circuit ("IC") including a charged device model ("CDM") clamp circuit connected to an input/output ("I/O") pad and to an interface circuit wherein the CDM clamp circuit and the interface circuit are adjacent to each other in addition to sharing a common device element. Claim 10 recites a method of protecting an IC from electrostatic discharge ("ESD") including the steps of disposing a CDM clamp circuit adjacent to an interface circuit and connected to an I/O pad and sharing a common device element between both the CDM clamp circuit and the interface circuit. Thus, Claims 1 and 10 both require a CDM clamp circuit adjacent to each other and sharing a common device element.

Claim 17 recites an IC comprising a semiconductor substrate and reciting devices including a drain region, a channel region, a source region and a gate overlying the channel region, wherein the devices share a source region. Claim 21 recites a method of forming an IC including the steps of forming two devices each including a drain region, a gate and a source region, wherein the devices share a source region.

By contrast, the patent to Pan apparently relates to an ESD protection circuit in which the ESD protection circuit is not adjacent to an interface circuit and does not share a common device element. Thus, with respect to Claims 1 and 10, note for example in Figure 3 of Pan that the two devices shown are devices 110 and 132, which correspond to devices 144 and 146, respectively, of Figure 4 of Pan. Those are the two ESD devices in Pan. The interface circuit of Pan comprises the two devices at the right of Figure 4 which are not even accorded reference numerals in Figure 4, and are not shown in Figure 3. Thus, in the patent to Pan, the ESD circuit clearly does not share a common device element with the interface circuit nor does Pan suggest such a configuration. In addition, by not even showing the interface circuit elements in either Figure 1 or Figure 3 and by saying nothing about their placement with respect to the ESD circuit elements, Pan clearly fails to teach or suggest that such circuits should be placed adjacent to one another. In fact, Pan is concerned about using parasitic capacitors to turn on parasitic bipolar junction transistors speedily, not with reducing or eliminating parasitic resistance and inductance from a metal interconnect system providing the connections between an ESD circuit and an interface circuit, as are Claims 1 and 10.

With respect to Claims 17 and 21, as mentioned in the previous paragraph, the patent to Pan clearly fails to teach or suggest devices sharing any element, much less sharing a source region.

Therefore, for the reasons set forth hereinabove, it is respectfully submitted that Claims 1, 10, 17 and 21 are allowable over the patent to Pan. The other claims subject to this rejection depend, either directly or indirectly, from either Claim 1 or 10, and so are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 18, 22, 19-20 and 23-24 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Pan as applied to Claims 17 and 21 above, and further in view of the patent to Utsunomiya et al., this rejection is respectfully traversed. All of these claims depend, either directly or indirectly from either Claim 17 or Claim 21, both of which require devices sharing a source region. As discussed hereinabove, the patent to Pan neither shows nor suggests devices sharing any

element, much less sharing a source region. The patent to Utsiunomiya et al. fails to cure the deficiencies of Pan. Thus, the patent to Utsunomiya et al. apparently relates to a semiconductor device and method for manufacturing a semiconductor device having a silicon on insulator ("SOI") structure and having an SOI static electricity protection circuit. There is no discussion or suggestion in the patent to Utsiunomiya et al. of any devices sharing any element, much less sharing a source region. For example, Figure 1 of Utsiunomiya et al. shows an internal circuit 102 formed by a MOSFET 105 and an SOI static electricity protection circuit 101 formed by an N-channel MOSFET 104. Figure 4 shows a MOSFET configured as an SOI static electricity protection circuit, such as MOSFET 104 of Figure 1. However, the drain 202 of this circuit is merely connected somehow to the I/O pad 103. The action of the circuit shown in Figure 1 protects the internal circuit "connected to the input output pad 103" (col. 5, lines 55-56). Clearly, the internal circuit and the device/circuit shown in Figure 4 do not share any element, much less share a source region.

Therefore, for the reasons set forth hereinabove, it is respectfully submitted that Claims 17 and 21 are allowable over the patent to Pan in view of the patent to Utsiunomiya et al. As mentioned above, the claims subject to this rejection depend, either directly or indirectly, from either Claim 17 or 21, and so are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

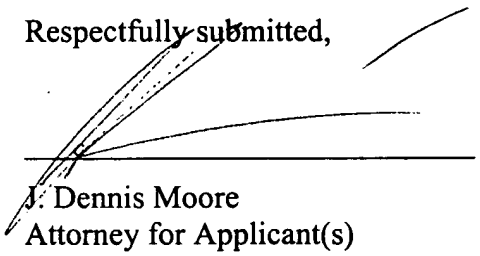
It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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